IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

DAVID R. HEMBREE
WARREN M. FARNWORTH
SALMAN AKRAM
ALAN G. WOOD
C. PATRICK DOHERTY
ANDREW J. KRIVY

Serial No.: Art Unit:

Division of Serial No. 09/929,388 filed August 14, 2001 Examiner

Filing Date: February 5, 2002

For: METHOD FOR TESTING SEMICONDUCTOR WAFERS (AS AMENDED)

Attorney Docket No. 96-750.3

PRELIMINARY AMENDMENT SUBMITTED WITH CONTINUING APPLICATION UNDER 37 CFR 1.53(b)

February 5, 2002

Assistant Commissioner of Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

Sir:

This Preliminary Amendment is being filed with a divisional application under 37 CFR 1.53(b). Please amend the captioned case as follows.

In the Drawings

Please substitute the attached new formal drawings for the drawings originally filed in parent application serial no. 08/797,719. The new formal drawings are also being submitted separately to the Official Draftsperson by "Transmittal Letter To The Official Draftsperson".

In the Specification

Please change the title to --Method For Testing Semiconductor Wafers--

On page 2, line 1, add the following:

--Cross Reference To Related Applications

This application is a division of application serial no. 09/929,388, filed August 14, 2001, which is a division of application serial no. 09/303,367 filed April 30, 1999, Patent No. 6,275,052, which is a division of application serial no. 08/797,719 filed February 11, 1997, Patent No. 6,060,891--

Please substitute the following clean replacement paragraph for the last paragraph on page 29 (page 29, line 29 to page 30, line 5).

--Following blanket deposition of the desired conductive metal, a resist mask can be formed and used for etching the conductive metal such that at least a portion of the contact members 20 remain covered with the conductive layers 52. The resist mask can be deposited using a standard photoresist deposition and exposure process. This can include spin deposition, followed by hardening, exposure and development. U.S. Patent Application Serial No. 08/520,871, now U.S. Patent No. 5,607,818, incorporated herein by reference describes a method for patterning a conductive layer using an electrophoretically deposited layer of resist.--

In the Claims

Please cancel claims 1-43 and 54-73.

Please amend claims 44-53, and add claims 74-90. Following is clean version of amended claims 44-53, and added claims 74-90, which represents all of the pending claims. In addition, a marked version of the amended claims follows the Remarks section of this Amendment.

Clean Version Of Amended And Added Claims

44. (amended) A method for testing a semiconductor wafer having a plurality of contact locations comprising:

providing a testing apparatus for handling the wafer and a test circuitry for applying test signals to the wafer;

providing a substrate comprising a plurality of contact members comprising raised members with penetrating projections configured to make temporary electrical connections with the contact locations;

bonding a membrane to the substrate and to the testing apparatus, the membrane configured to provide an electrical path between the contact members and the test circuitry and to suspend the substrate to the testing apparatus such that the substrate and the contact members can move for making the electrical connections;

biasing the substrate against the wafer to make the electrical connections; and

applying test signals through the membrane and the contact members to the contact locations.

45. (amended) The method of claim 44 wherein the contact members make the electrical connections with each die on the wafer at a same time and the test signals are electronically switched to selected dice.

46. (amended) The method of claim 44 wherein the membrane allows the substrate to freely move in a z-direction.

47. (amended) The method of claim 44 wherein the membrane comprises an electrically insulating tape and a plurality of conductors on the tape.

48. (amended) A method for testing a semiconductor wafer having a plurality of bumped contact locations comprising:

providing a testing apparatus configured to handle the wafer and a test circuitry configured to apply test signals to the wafer;

providing a substrate comprising a plurality of contact members comprising conductive indentations configured to retain and make temporary electrical connections with the bumped contact locations;

bonding a membrane to the substrate and to the testing apparatus comprising a polymer tape and a plurality of conductors on the polymer tape configured to provide electrical paths between the contact members and the test circuitry, the membrane suspending the substrate on the testing apparatus with a slack sufficient to permit movement of the substrate and the contact members in a z-direction for making the electrical connections;

biasing the substrate against the wafer to make the electrical connections; and

applying the test signals through the conductors and the contact members to the contact locations.

49. (amended) The method of claim 48 wherein the polymer tape comprises polyimide and the conductors comprise copper.

50. (amended) The method of claim 48 wherein the substrate comprises silicon.

51. (amended) A method for testing a semiconductor wafer containing a plurality of semiconductor dice with a plurality of contact locations comprising:

providing a testing apparatus configured to handle the wafer and a testing circuitry configured to apply test signals to the wafer;

providing a probe card comprising a substrate, a raised contact member on the substrate at least partially covered with a conductive layer, and a conductor on the substrate in electrical communication with the conductive layer, the raised contact member having a height on the substrate of from 10μm to 100μm, the raised contact member comprising a surface and a penetrating projection on the surface with a height of from .1μm to 1μm configured to penetrate a contact location on the wafer to a limited penetration depth;

providing a membrane comprising a polymer tape and a conductor on the tape;

physically and electrically connecting the probe card to the testing apparatus using the membrane, with the probe card movable in a z-direction on the testing apparatus;

placing the probe card on the wafer to make a temporary electrical connection between the contact location and the contact member with the probe card moving in the z-direction; and

applying the test signals through the conductor and the contact member to the contact locations.

52. (amended) The method of claim 51 further comprising mounting a compressible member to the probe card for cushioning contact forces.

53. (amended) The method of claim 52 further comprising applying pressure from the testing apparatus to

the probe card using a pressure plate in contact with the compressible member.

74. (added) A method for testing a semiconductor wafer having a plurality of contact locations comprising:

providing a mounting plate comprising a sealed space;

providing a substrate comprising a plurality of contact members configured to electrically contact the contact locations;

slidably mounting the substrate within the sealed space

providing a gas supply in flow communication with the sealed space configured to exert a biasing force on the substrate;

applying the biasing force to the substrate using the sealed space and the gas supply to make a plurality of temporary electrical connections between the contact members and the contact locations; and

applying test signals through the contact members to the contact locations.

75. (added) The method of claim 74 further comprising providing a leveling mechanism and leveling the substrate with respect to the wafer using the leveling mechanism.

76. (added) The method of claim 74 wherein the test signals are applied through a membrane attached to the substrate.

77. (added) A method for testing a semiconductor wafer having a plurality of contact locations comprising:

providing a testing apparatus in electrical communication with a test circuitry configured to apply test signals to the wafer;

providing a mounting plate on the testing apparatus comprising a plurality of pads and a plurality of conductors in electrical communication with the pads;

providing a substrate on the mounting plate comprising a plurality of contact members in electrical communication with the conductors configured to electrically contact the contact locations on the wafer;

providing a plurality of spring loaded electrical connectors on the testing apparatus in electrical communication with the test circuitry and in physical and electrical contact with the pads on the mounting plate;

biasing the substrate against the wafer using a biasing force applied by the electrical connectors; and

applying test signals through the electrical connectors and the contact members to the contact locations.

78. (added) The method of claim 77 wherein the pads are arranged in a grid array.

79. (added) The method of claim 77 wherein the electrical connectors comprise pogo pins.

80. (added) The method of claim 77 wherein each contact member comprises a raised member comprising a surface and a projection on the surface configured to penetrate a contact location on the wafer.

81. (added) The method of claim 77 wherein each contact member comprises an indentation in the substrate at least partially covered by a conductive layer.

82. (added) The method of claim 77 wherein the testing apparatus comprises a wafer prober.

83. (added) A method for testing a semiconductor wafer having a plurality of contact locations comprising:

providing a testing apparatus configured to handle the wafer;

providing a test circuit configured to apply test signals to the wafer;

providing a probe card on the testing apparatus comprising a plurality of pads and a plurality of contact members in electrical communication with the pads configured to make temporary electrical connections with the contact locations on the wafer;

providing a plurality of spring loaded electrical connectors on the testing apparatus in electrical communication with the test circuit;

placing the electrical connectors in physical and electrical contact with the pads and applying a biasing force through the probe card to the wafer to make the temporary electrical connections; and

applying the test signals through the electrical connectors and the contact members to the contact locations.

84. (added) The method of claim 83 wherein the probe card comprises a mounting plate wherein the pads are contained.

85. (added) The method of claim 84 further comprising providing a compressible member between the mounting plate and the substrate configured to cushion the biasing force.

86. (added) The method of claim 83 wherein the contact members comprises pins having spring segments.

87. (added) The method of claim 83 wherein the contact members comprise raised members having projections for penetrating the contact locations.

88. (added) The method of claim 83 wherein the contact locations comprise bumps and the contact members comprise depression at least partially covered by conductive layers.

89. (added) The method of claim 83 wherein the testing apparatus comprises a wafer prober.

90. (added) The method of claim 83 wherein the probe card comprises a silicon substrate and the contact members comprise silicon projections on the substrate.

REMARKS

By this Amendment, claims 1-43 and 54-73 have been canceled, claims 44-53 have been amended, and claims 74-90 have been added.

Amended claims 44-53 are directed to a test method using a probe card 10 configured as shown in Figures 5 and 5A, with a flexible membrane 18.

Added claims 74-76 are directed to a test method using a probe card configured as shown in Figure 7D, with a slidable mounting plate 80A.

Added claims 77-90 are directed to a test method using a probe card configured as shown in Figure 7B, with spring loaded electrical connectors 42 for applying a biasing force and test signals.

Also being submitted with this divisional application are copies of a Petition for Correction of Inventorship in parent application serial no. 08/797,719, along with accompanying documents, and a Decision granting the Petition. In addition, an Information Disclosure Statement is being submitted with this divisional application.

Favorable consideration and allowance of amended claims 44-53 and added claims 74-90 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 5th day of February, 2002.

Respectfully submitted:

Stephen A. Gratton
Registration No. 28,418
Attorney for Applicants

2764 S. Braun Way
Lakewood, CO 80228
Telephone: (303) 989-6353
FAX (303) 989-6538

Marked Version Of Specification Showing Changes

On page 30, line 2, after "Application Serial No. 08/520,871" add, --now, U.S. Patent No. 5,607,818--.

Marked Version Of Claims Showing Changes

44. (amended) A method for testing a semiconductor wafer having a plurality of contact locations comprising:

providing a testing apparatus for handling the wafer [comprising a force applying mechanism] and a test circuitry for applying test signals to the wafer;

providing a substrate comprising a plurality of contact members comprising raised members with penetrating projections configured to [establish] make temporary electrical [communication with] connections with the contact locations; [on the wafer, said contact members comprising raised members with penetrating projections;]

bonding a membrane to the substrate and to the testing apparatus, [said] the membrane configured to provide an electrical path [to] between the contact members and the test circuitry and to [mount] suspend the substrate to the testing apparatus such that the substrate and the contact members can move for making the electrical connections;

biasing the substrate against the wafer to make the electrical connections; and

applying test signals through the membrane and the contact members to the contact locations. [on the wafer.]

45. (amended) The method [as claimed in] of claim 44 [and] wherein the [substrate includes] contact members [for contacting] make the electrical connections with each die on the wafer at a same time and the test signals are electronically switched to selected dice.

46. (amended) The method [as claimed in] of claim 44 wherein the membrane allows the substrate to freely move in a z-direction.

[and further comprising mounting a compressible member between the force applying mechanism and substrate.]

47. (amended) The method [as claimed in] of claim 44 [and] wherein the membrane comprises an electrically insulating tape [having] and a plurality of conductors on the tape.

[and microbumps for bonding to the substrate.]

48. (amended) A method for testing a semiconductor wafer having a plurality of bumped contact locations comprising:

providing a testing apparatus configured to handle the wafer [comprising a force applying mechanism] and a test circuitry configured to apply test signals to the wafer;

providing a substrate comprising [indentation] a plurality of contact members comprising conductive indentations configured to retain [bumped contact locations on the wafer and to establish] and make temporary electrical [communication] connections with the bumped contact locations;

bonding a membrane to the substrate and to the testing apparatus comprising a polymer tape and a plurality of conductors on the polymer tape [, said membrane] configured to provide [an] electrical paths between [to] the contact members and the test circuitry, [to mount] the membrane suspending the substrate [to] on the testing apparatus with a slack sufficient to permit movement of the substrate and the contact members in a z-direction for making the electrical connections;

biasing the substrate against the wafer to make the electrical connections; and

applying the test signals through the [membrane] conductors and the contact members to the contact locations. [on the wafer.]

49. (amended) The method [as claimed in] of claim 48 wherein the polymer tape comprises polyimide and the conductors comprise copper.
[and further comprising mounting a compressible member to a backside of the substrate for cushioning a pressure applied to the substrate by the force applying mechanism.]

50. (amended) The method [as claimed in] of claim 48 [and] wherein the substrate comprises silicon.

51. (amended) A method for testing a semiconductor wafer containing a plurality of semiconductor dice with a plurality of contact locations comprising:

providing a testing apparatus configured to handle the wafer and a testing circuitry configured to apply test signals to the wafer;

providing a probe card comprising a substrate, [with] a raised contact member on the substrate at least partially covered with a conductive layer, and a conductor on the substrate in electrical communication with [a conductor, said] the conductive layer, the raised contact member having a height on the substrate of from 10μm to 100μm, [and having] the raised contact member comprising a surface and a penetrating projection [formed thereon] on the surface with a height of from .1μm to 1μm [, said projection] configured to penetrate a contact location on the wafer to a limited penetration depth;

providing a membrane comprising a polymer tape and a conductor on the tape;

physically and electrically connecting the probe card to [a] the testing apparatus using [a] the membrane, with the probe card movable in a z-direction on the testing apparatus;

[having a second conductor bonded to the conductor on the substrate; and]

placing the probe card on the wafer to make a temporary electrical connection between the contact location and the contact member with the probe card moving in the z-direction; and

applying the test signals through the [second] conductor [, through the conductor, and through the contact member to] and the contact member to the contact locations.

52. (amended) The method [as claimed in] of claim 51 [and] further comprising mounting a compressible member to the probe card for cushioning contact forces. [between the force applying mechanism and substrate.]

53. (amended) The method [as claimed in] of claim [51] 52 [and] further comprising applying pressure from the testing apparatus [through] to the probe card using a pressure plate in contact with the compressible member.

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February 5, 2002
Date of Signature

Stephen A. Gratton, Attorney for Applicants

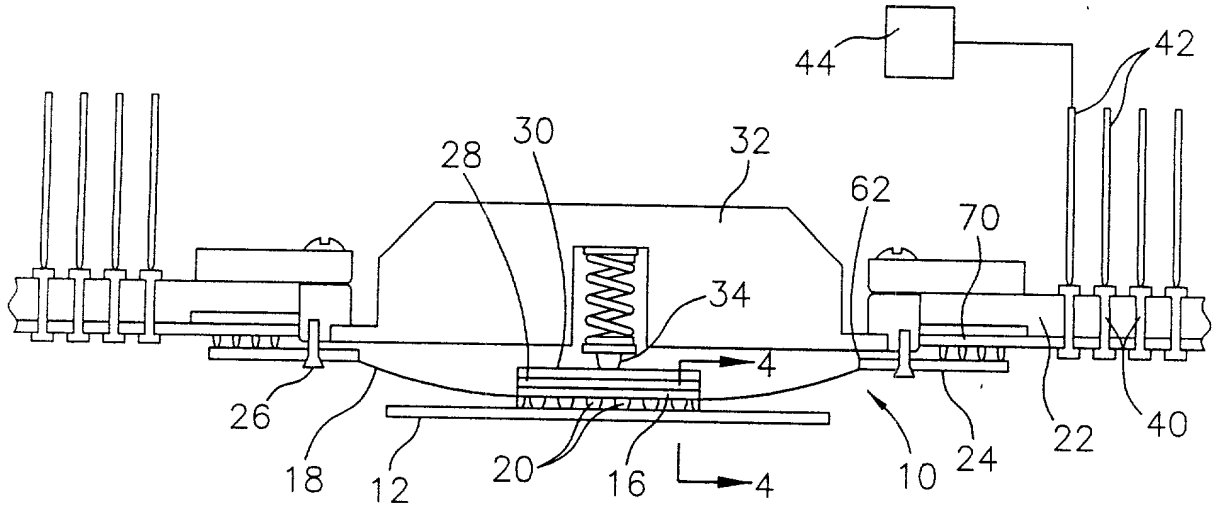

FIGURE 1

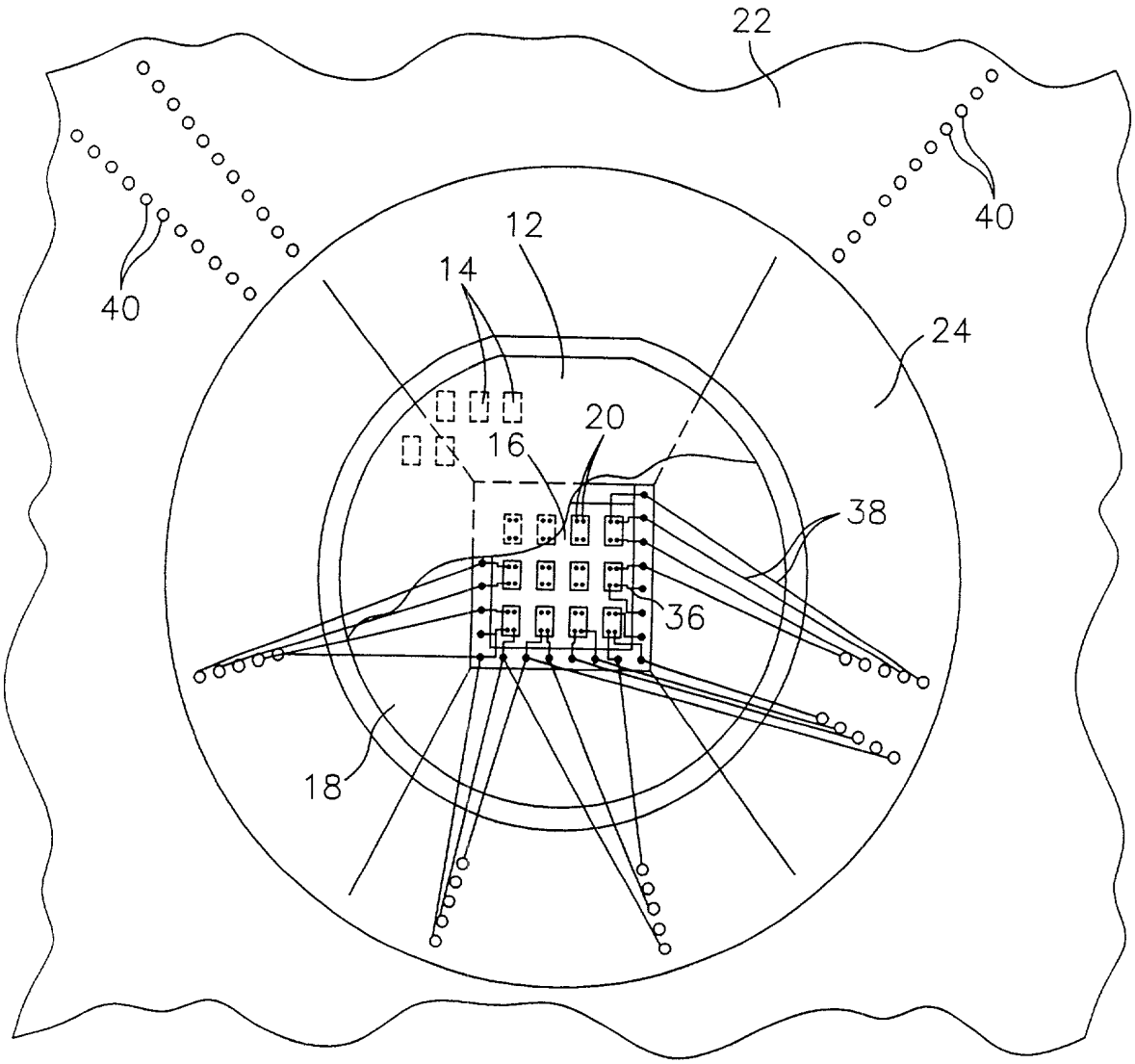

FIGURE 2

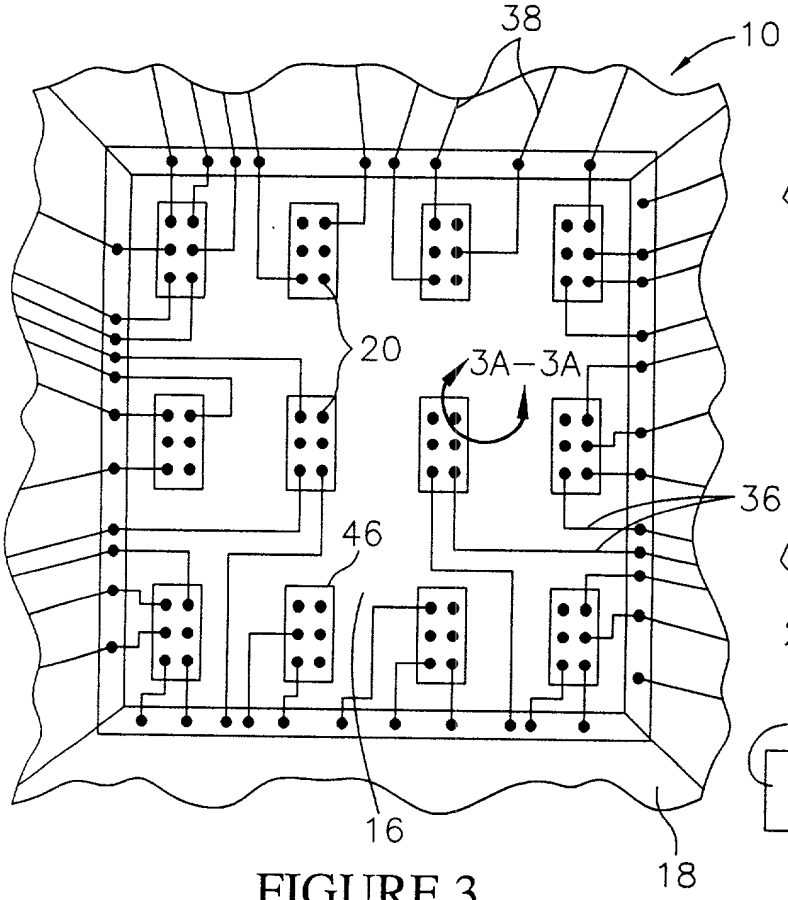

FIGURE 3

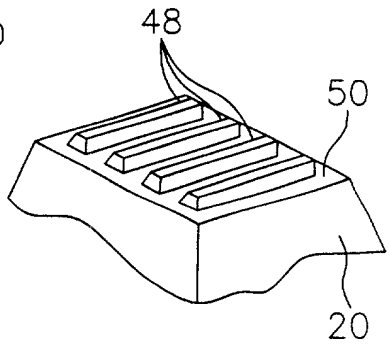

FIGURE 3A

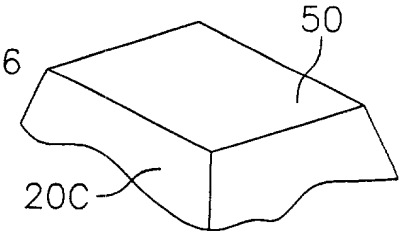

FIGURE 3B

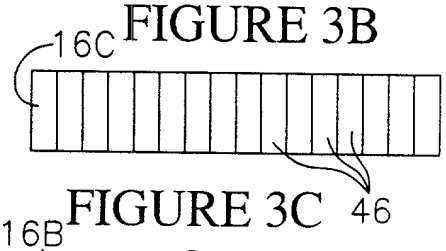

FIGURE 3C

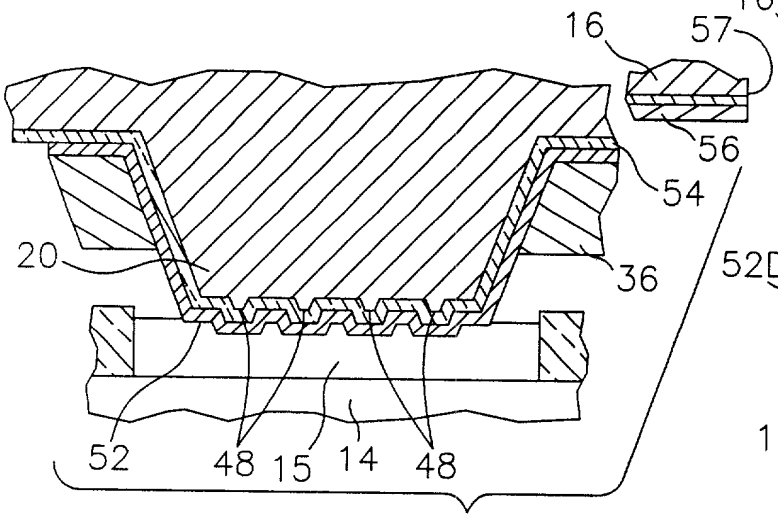

FIGURE 4

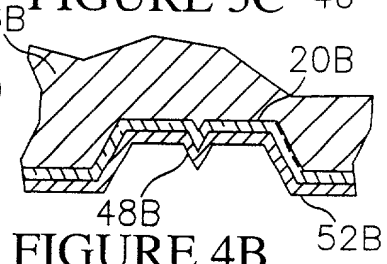

FIGURE 4B

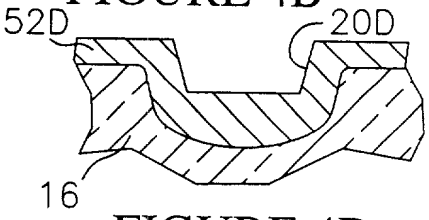

FIGURE 4D

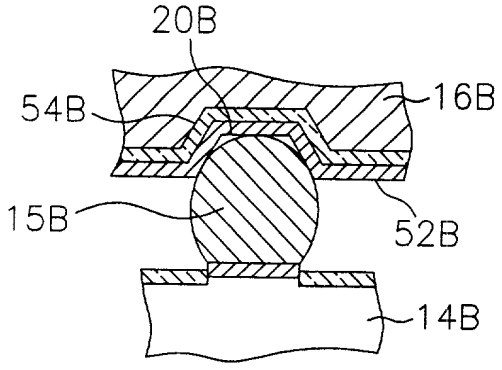

FIGURE 4A

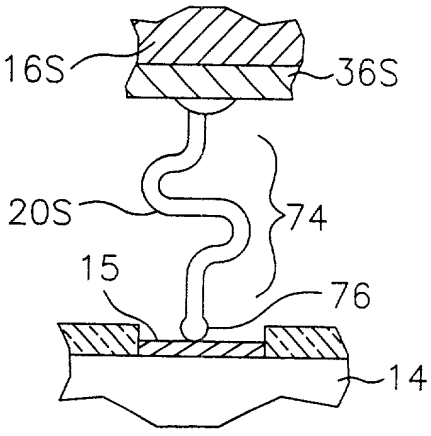

FIGURE 4C

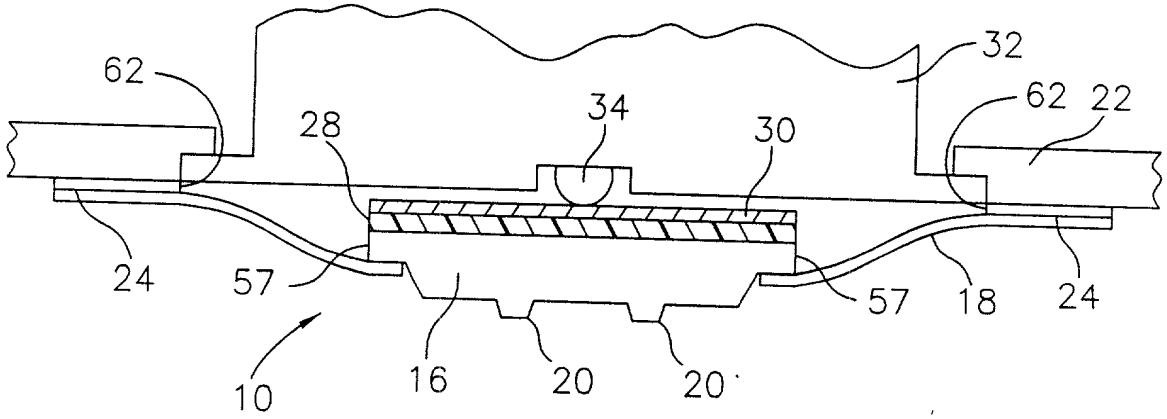

FIGURE 5

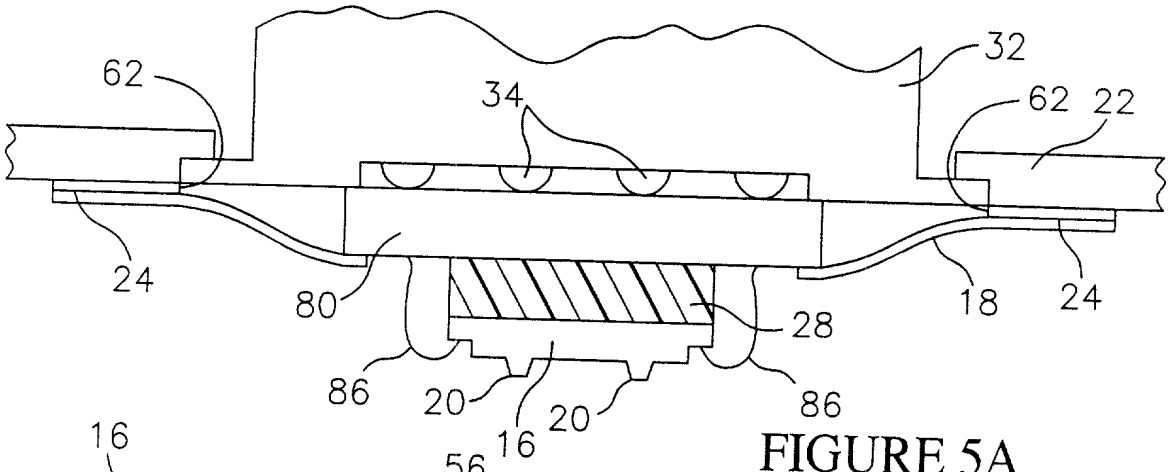

FIGURE 5A

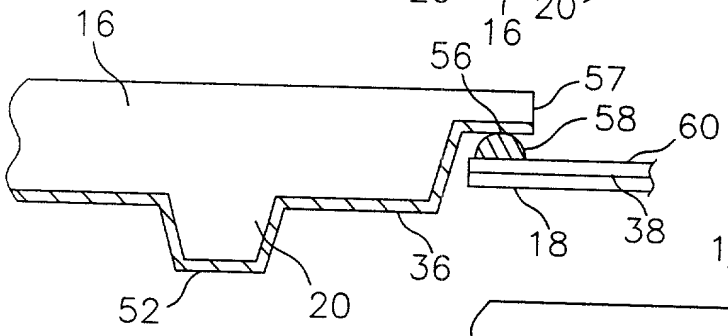

FIGURE 6A

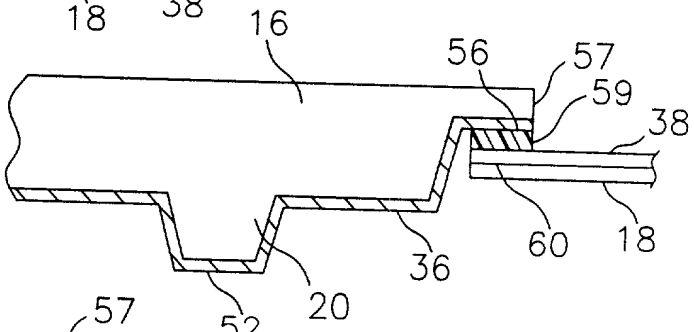

FIGURE 6B

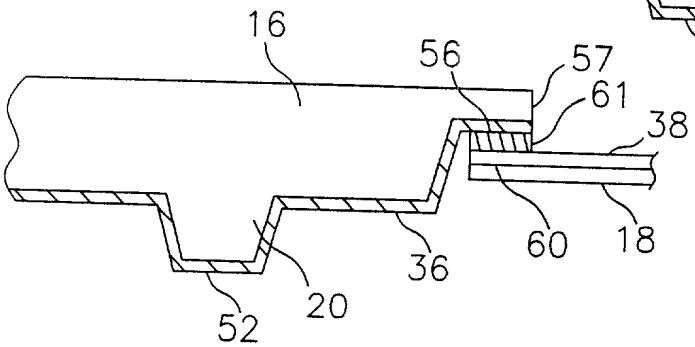

FIGURE 6C

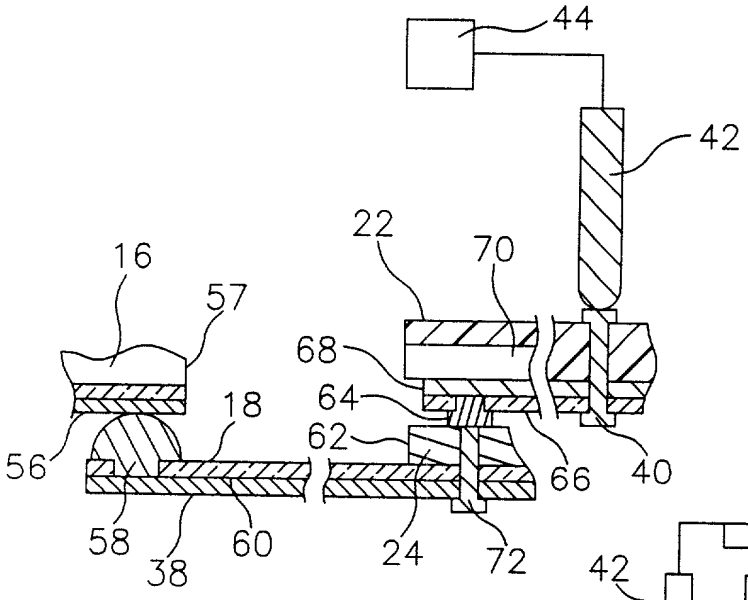

FIGURE 7A

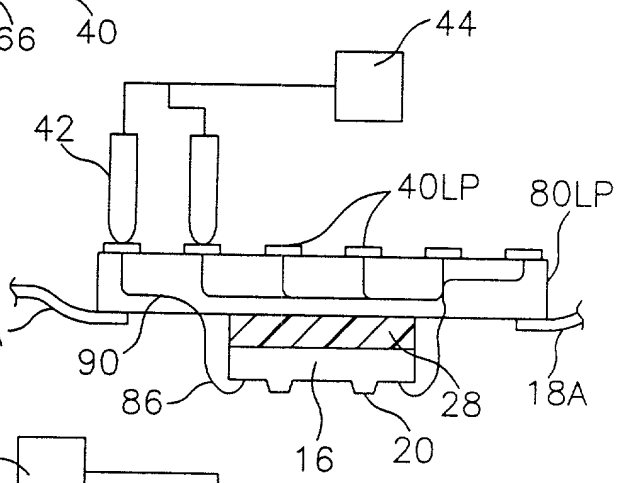

FIGURE 7B

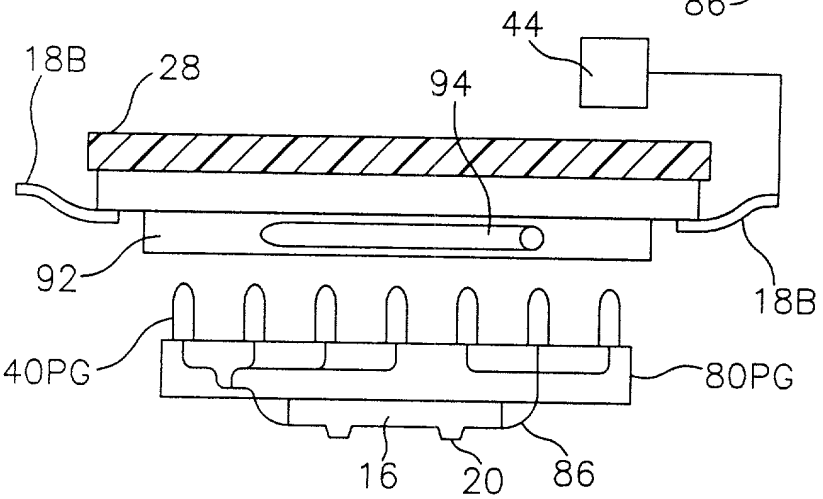

FIGURE 7C

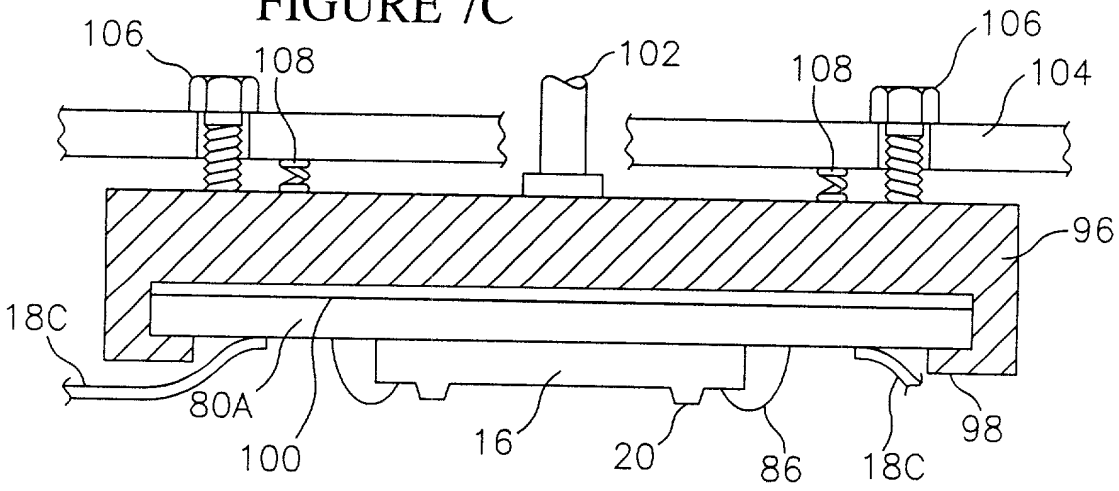

FIGURE 7D

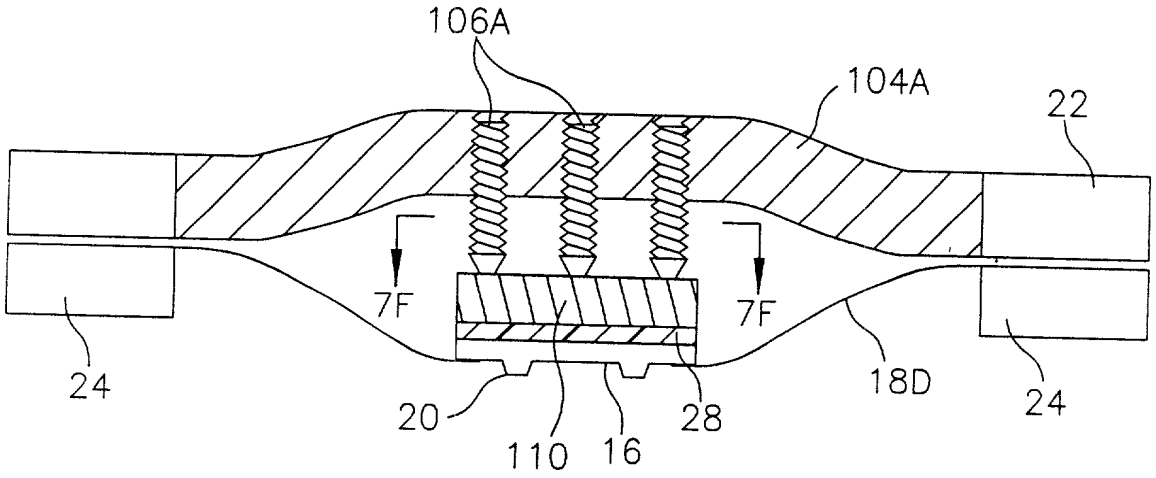

FIGURE 7E

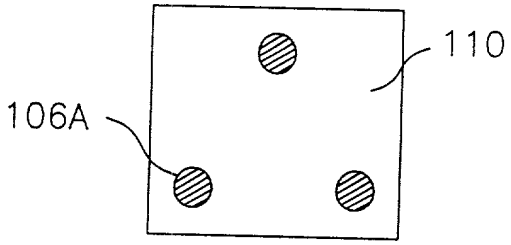

FIGURE 7F

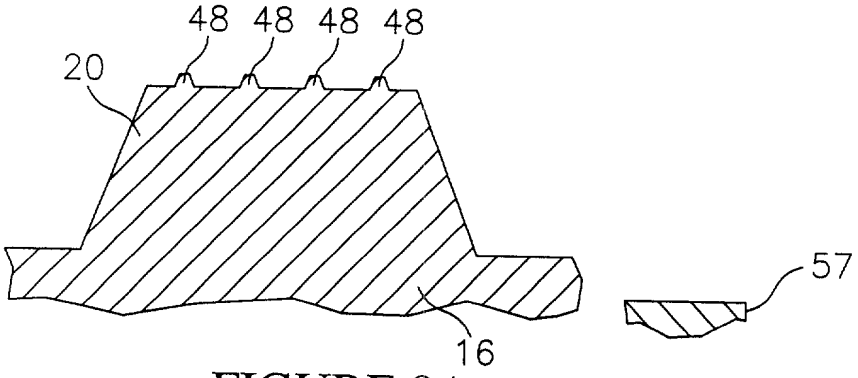

FIGURE 9A

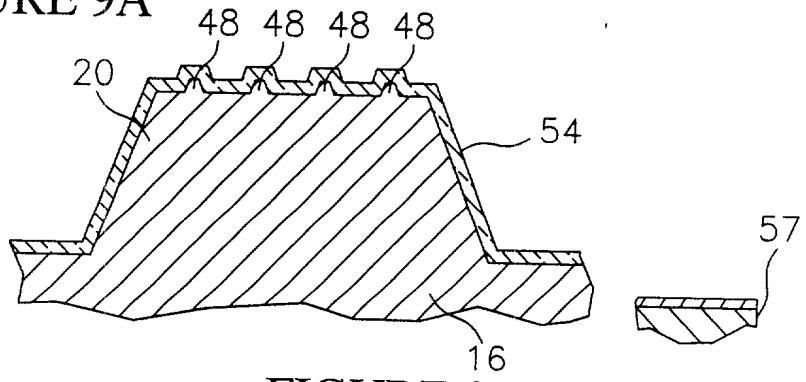

FIGURE 9B

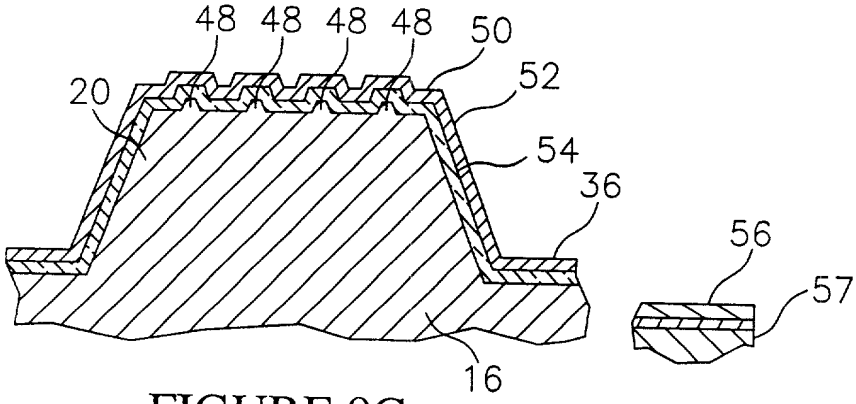

FIGURE 9C

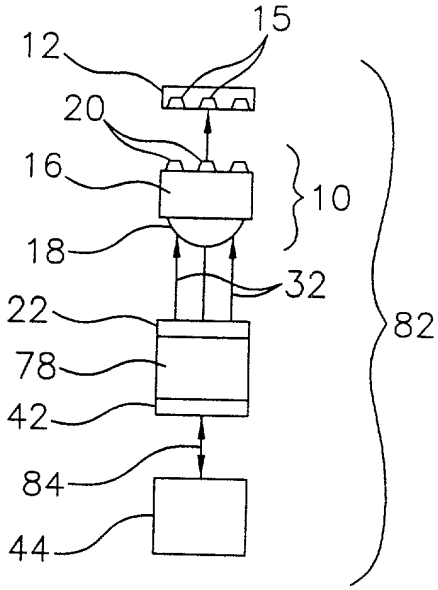

FIGURE 8